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Harmonic-Recycling Rectification Based on Novel Compact Dual-Band Resonator

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***Abstract*—Harmonic generation during radio frequency (RF)-dc conversion causes performance degradation of a microwave rectifying circuit. To suppress and recycle the harmonic power, this letter proposes a novel compact dual-band resonator (DBR) based on a microstrip coupled transmission line. It presents open-circuits at the second and third harmonic frequencies, which effectively block the higher order harmonic for power recycling. The conventional input cascading filters for harmonic rejection can be eliminated, simplifying the circuit topology and reducing loss. Theoretical analyses were carried out and corresponding equations were formulated for the proposed DBR. For validation, two rectifying circuits with/without the DBR operating at 2.2 GHz were fabricated and tested. Using the proposed DBR at 10 dBm RF power, the suppression of the second and third harmonic powers is enhanced by 18.4 and 7.6 dB, respectively. Besides, an improvement of RF-dc power conversion efficiency (PCE) was observed; specifically, PCE reached 73.2% at 10 dBm compared to 71.6% obtained from an equivalent rectifier.**

***Index Terms*—Dual-band resonator (DBR), harmonic-recycling, rectifying circuit, wireless power transmission.**

I. Introduction

MICROWAVE rectifying circuits, essential components in wireless power transfer (WPT) systems, play a crucial role in converting radio frequency (RF) power to dc power [1], [2], [3]. The overall efficiency of WPT systems heavily relies on the power conversion efficiency (PCE) of the rectifying circuit [4], [5], [6], [7]. Therefore, the primary requirement of a rectifying circuit is high RF–dc PCE, and miniaturization is another requirement for system integration in the antenna array.

In a rectifying circuit, the diode generates frequency harmonics from the incoming power, thereby reducing the proportion of energy converted to direct current and resulting in unwanted harmonic emissions. Moreover, as the incident RF energy increases, the energy lost to harmonics further increases [8], [9]. Consequently, recycling rectification of the harmonic power is an effective method to boost the PCE of a rectifying circuit.

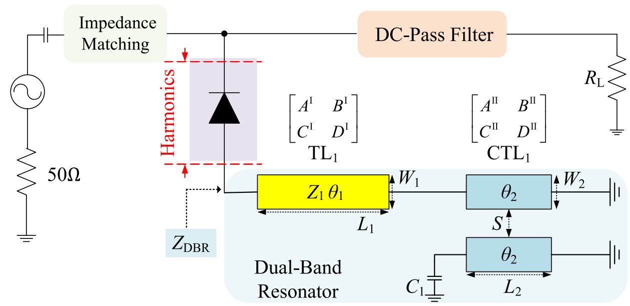

Fig. 1. Microwave rectifying circuit using a DBR for harmonic recycling.

Filtering of the harmonics at both the input and output has been investigated, as shown in [10] and [11], mainly to reduce reradiated harmonic power. Usually, filters, e.g., band-stop [12], or low-pass filter [13] are applied between the diodes and the input/output of the microwave rectifier to reflect harmonics produced during rectifying, and the reflected harmonics go back to the diode where they can be converted to dc. It is noticed that the filters at the input raise a concern about the insertion loss and circuit area.

Class-F loads and harmonically terminated techniques are alternatives to the low-pass or dc-pass of rectifiers [14], it has good potential applications for high-frequency microwave rectifiers. Diode rectifiers using Class-C loads [15], [16] and a 5.8-GHz charge pump rectifier with Class-F loads [17] demonstrated an improvement in PCE. In reality, the optimum impedance for harmonic-terminated operation is difficult to achieve as the package of the device has parasitics that move the harmonic impedances.

Recently, a competitive solution has emerged in the form of a compact serial bandstop structure. This innovative approach not only effectively blocks radiation of harmonics but also compensates for the diode capacitive impedance at the fundamental frequency [7], [18]. In [7], a short-ended eighth-wavelength microstrip transmission line was employed to impede the second harmonic and enhance power recycling. However, solely the second harmonic can be recycled.

In this letter, we propose a novel harmonic suppression structure using a dual-band resonator (DBR) to efficiently recycle both the second and third harmonic power with a compact circuit topology. The DBR is based on our previous work [19], where we found that a microstrip line in serial with a coupled pair of microstrip-lines could provide two

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poles (open-circuits) for impeding harmonic radiation. In this letter, we further investigate this structure as a DBR to demonstrate its ability to block the second and third harmonics for enhanced power recycling compared to [7]. With the proposed DBR, a simple and compact circuit structure was realized, resulting in a decrease in insertion loss and an improvement of PCE.

II. Principle and Design Method

A. Principle

As shown in Fig. 1, owing to the high impedance provided by the harmonic suppression structure, high-order harmonics are confined to the diode without returning to the input port, thus the conversion efficiency of a rectifying circuit can be improved. However, in this design, the harmonic suppression structure in series with the diode has been realized through a DBR which is placed between the diode and the ground plane. A DBR in series with the diode should have the following functions.

1) Presenting a short circuit at dc, which provides a dc path for the rectifying circuit output.
2) Compensating the capacitive impedance of the diode, which facilitates the impedance matching circuit of the rectifying circuit.
3) Exhibiting high reflections at harmonic frequencies $nf_0 (n = 2, 3)$, which blocks them from returning the input port.

Fig. 1 shows a rectifying circuit operating with a DBR for harmonic recycling, it has three parts: 1) a quarter-wave transformer, which may be needed for the impedance matching at f_0; 2) a dc-pass filter to prevent RF signals from entering the load; and 3) a DBR, employed to recycle the second and third harmonic power through rectifying or mixing with other frequencies.

B. Proposed DBR

Based on the above analysis, the input impedance of the proposed DBR for harmonic recycling can be expressed as

$$\begin{cases} Z_{\mathrm{DBR}}@\mathrm{dc} = 0 \\ Z_{\mathrm{DBR}}@f_0 = jX_L \\ Z_{\mathrm{DBR}}@2f_0 = \infty \\ Z_{\mathrm{DBR}}@3f_0 = \infty. \end{cases} \tag{1}$$

A practical microstrip band-stop structure to block the third harmonics is a short-ended $\lambda/12$ transmission line. Inspired by this idea, a small section of a short-ended $\lambda/12$ transmission line is modified with a coupled transmission line (CTL_1), which is shown in Fig. 1. Due to the odd and even modes of the CTL_1, besides the third harmonic, another resonant frequency at the second harmonic can be simultaneously obtained.

Fig. 1 shows the schematic of the proposed DBR. The impedance and electrical length of TL_1 are Z_1 and θ_1, respectively, thus its ABCD matrix [20] is

$$\begin{bmatrix} A^{\mathrm{I}} & B^{\mathrm{I}} \\ C^{\mathrm{I}} & D^{\mathrm{I}} \end{bmatrix} = \begin{bmatrix} \cos\theta_1 & jZ_1\sin\theta_1 \\ j\dfrac{\sin\theta_1}{Z_1} & \cos\theta_1 \end{bmatrix}. \tag{2}$$

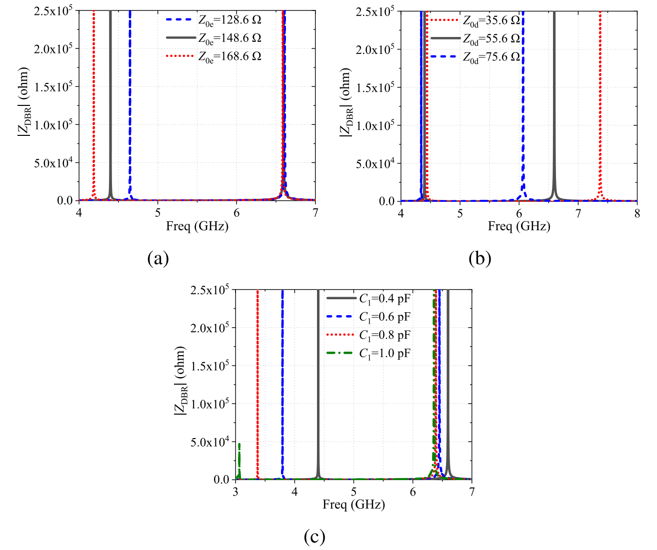

Fig. 2. Calculated $|Z_{\mathrm{DBR}}|$ versus RF frequency with perturbation of (a) Z_{0e}, (b) Z_{0d}, and (c) C_1.

Width W_2 and gap S determine the even and odd-mode impedance of CTL_1, Z_{0e}/Z_{0d}. The ABCD matrix of CTL_1 can be expressed as

$$\begin{bmatrix} A^{\mathrm{II}} & B^{\mathrm{II}} \\ C^{\mathrm{II}} & D^{\mathrm{II}} \end{bmatrix} = \begin{bmatrix} \dfrac{Z_{0e}+Z_{0d}}{Z_{0e}-Z_{0d}} & j\dfrac{2\tan\theta_2}{(Z_{0e}-Z_{0d})} \\ -j\dfrac{2\cot\theta_2}{Z_{0e}-Z_{0d}} & \dfrac{Z_{0e}+Z_{0d}}{Z_{0e}-Z_{0d}} \end{bmatrix}. \tag{3}$$

Cascading the ABCD matrices in (2) and (3) leads to

$$\begin{bmatrix} A^{\mathrm{III}} & B^{\mathrm{III}} \\ C^{\mathrm{III}} & D^{\mathrm{III}} \end{bmatrix} = \begin{bmatrix} A^{\mathrm{I}} & B^{\mathrm{I}} \\ C^{\mathrm{I}} & D^{\mathrm{I}} \end{bmatrix} \times \begin{bmatrix} A^{\mathrm{II}} & B^{\mathrm{II}} \\ C^{\mathrm{II}} & D^{\mathrm{II}} \end{bmatrix}. \tag{4}$$

Finally, the input impedance of the proposed DBR, with one port terminated in C_1, is

$$Z_{\mathrm{DBR}} = \frac{A^{\mathrm{III}}Z_C + B^{\mathrm{III}}}{C^{\mathrm{III}}Z_C + D^{\mathrm{III}}} \tag{5}$$

where Z_C is the impedance of capacitor C_1.

To verify the input impedance calculation and the performance of the proposed DBR, numerical experiments were carried out for a DBR operating at a fundamental frequency of 2.2 GHz. Considering the fabrication precision of PCB manufacture, the default width W_2 and gap S of CTL_1 are 0.3 and 0.2 mm, respectively. Since TL_1 is in series with CTL_1, its width W_1 stays the same as W_2. Thus, the initial parameters of DBR are $Z_1 = 107.6\ \Omega$, $Z_{0e} = 148.6\ \Omega$, and $Z_{0d} = 55.6\ \Omega$ with an RF laminate RO4350B of 0.76-mm thickness. When C_1 is 0.4 pF, θ_1 and θ_2 are calculated as 15.9° and 18.6°, respectively. Substituting the above parameters into (5) for calculation, Fig. 2 shows the calculated $|Z_{\mathrm{DBR}}|$ with perturbation of Z_{0e}, Z_{0d}, and C_1, respectively.

The frequency response of the DBR was studied through sweeping each parameter individually. As shown in Fig. 2(a), the first pole of $|Z_{\mathrm{DBR}}|$ shifts to the left side dynamically with an increase of Z_{0e}, whereas the second pole of $|Z_{\mathrm{DBR}}|$ moves to the right side rapidly with a decrease of Z_{0d} [see Fig. 2(b)]. Regarding the influence of capacitor C_1, Fig. 2(c) illustrates the shift in $|Z_{\mathrm{DBR}}|$ as C_1 increases toward infinity (effectively a short circuit), with the other parameters remain the same as those in Fig. 2(a). It is observed the second pole of $|Z_{\mathrm{DBR}}|$

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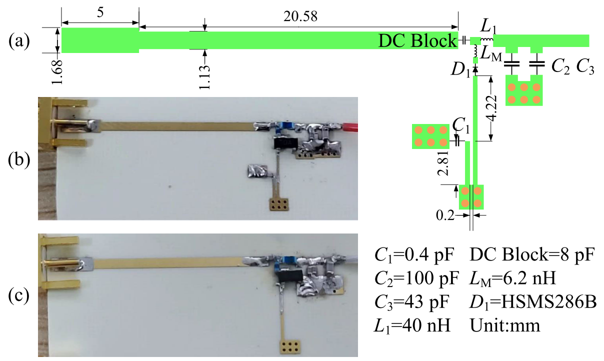

Fig. 3. (a) Circuit layout with design parameters for the proposed DBR. (b) Rectifying circuit with the proposed DBR. (c) Rectifying circuit without harmonic recycling for performance comparison.

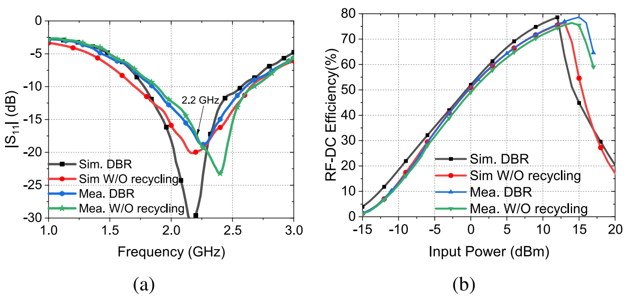

Fig. 4. (a) Simulated and measured $|S_{11}|$ versus RF frequency at 10-dBm input power and (b) PCE versus RF input power.

stays the same place because C_1 is equivalent to a short circuit at a relatively high frequency, whereas the first pole shifts toward lower frequencies as C_1 increases. As a result, the first pole can be tuned through C_1. However, a large C_1 may place the first pole very close to f_0, which should be avoided.

III. Implementation and Measurement

A rectifying circuit operating at $f_0 = 2.2$ GHz was simulated in advanced design system (ADS, Keysight) with physical dimensions indicated in Fig. 3, and the RO4350B ($\epsilon_r = 3.66$ and $\tan\delta = 0.002$) was used. L_M is a chip inductor for compensating the capacitive impedance of the diode. Fig. 3 shows a photograph of the fabricated rectifying circuit. For performance comparison, a rectifying circuit without harmonic recycling was also fabricated.

The measured reflection coefficient $|S_{11}|$ at the input power of 0 and 10 dBm are shown in Fig. 4(a). For the rectifying circuit with the DBR, $|S_{11}|$ curve for 10 dBm is well below -10 dB for frequencies ranging from 1.85 to 2.6 GHz. It is observed that $|S_{11}|$ for rectifying circuits with/without the DBR are almost the same.

Fig. 4(b) depicts the simulated measured PCE versus input power at 2.2 GHz and 400 Ω dc load. As observed at 10 dBm, the measured PCE of the rectifying circuits with/without the proposed DBR are 73.2% and 71.6%, respectively, while simulated PCE for both rectifiers are 76.2% and 73.4%, respectively. Because the measured $|S_{11}|$ versus input power are not same for both rectifiers, the improvement of PCE by the measurement is lower than that of the simulation. Compared to the reference rectifier, the rectifying circuit using the proposed DBR shows an improvement in PCE at high input power levels (0–14 dBm).

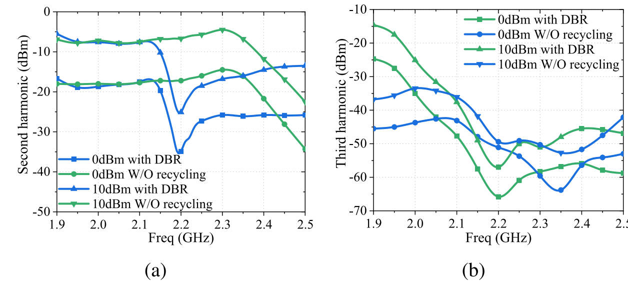

Fig. 5. Measured harmonic power versus RF frequency at 0- and 10-dBm input power. (a) Second harmonic. (b) Third harmonic.

TABLE I
Performance Comparison of Harmonic-Recycling Rectifiers

Ref.	[7]	[18]	[21]	This work
Freq (GHz)	2.45	2.45	2.6	2.2
PCE (%)	80.9	80.2	47	78.6
Pow.(dBm)	20	25	0	15
Diode	HSMS-282	HSMS-282	HSMS-2850,2860	HSMS-286B
Size (mm)	16 × 18	20 × 5	37 × 31	34 × 11
Size (λ_g^2)	0.051	0.018	0.219	0.073
Technology	TL. $\lambda/8$ short-ended	TL. $\lambda/8$ short-ended	Another rectifier cell	Dual-band resonator
Harmonic Supp. (dB)	N.A	N.A	N.A	18.4@$2f_0$ 7.6@$3f_0$
Diode Num.	1	2	2	1

The measured power levels of the second and third harmonic are depicted in Fig. 5(a) where the rectifying circuit with DBR presents an obvious low point at 2.2 GHz. Specifically, at 10 dBm, the suppression of the second harmonic is enhanced from -6.7 to -25.1 dBm by the proposed DBR (an improvement of 18.4 dB). Meanwhile, as shown in Fig. 5(b), the rectifying circuit with DBR demonstrates better control over the third harmonic, showing an improvement of 7.6 dB by comparison. The measured harmonic power versus frequency validates the effectiveness of harmonic control through the proposed DBR.

Table I shows a comparison of the performances between the proposed rectifying circuit and those reported in the literature targeting harmonic recycling. As shown, the rectifying circuit using the proposed DBR has demonstrated the effectiveness of harmonic control over the second and third harmonics, while harmonic suppressions in other references were not reported. Meanwhile, only one diode is used, which helps to minimize the losses associated with the diode turn-on voltage.

IV. Conclusion

A novel compact DBR has been developed for recycling the second and third harmonic power in a microwave rectifying circuit. It functions as both a filter and an inductor for impedance matching, the conventional input cascading bandpass or low-pass filters for harmonic rejection can be eliminated, leading to a simple circuit topology with low loss. Compared to a reference rectifier, the proposed DBR demonstrates better control over the second and third harmonic, showing an improvement of 18.4 and 7.6 dB, respectively. Besides, improved PCEs at high input power levels were also observed.

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